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SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

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Patent Claims

Claim 1

A semiconductor device characterized by the possession of

A first electroconductor filled into and formed within the interior of a wire channel formed above a semiconductor substrate,

A capacitor for an anti-fuse constituted not only to bear an upper metal electrode/insulating film/lower metal stack structure formed above the aforementioned first electroconductor but also to become writable as a result of the electric contact of the aforementioned lower metal with the aforementioned first electroconductor and then of the electric insulation breakdown of the aforementioned insulating film, and

A pair of second electroconductors formed respectively above the aforementioned first electroconductor and above said capacitor in such a way that they will become contacted respectively with the aforementioned first electroconductor and the upper metal electrode of the aforementioned capacitor.

Claim 2

A semiconductor device characterized by the possession of

A first electroconductor for a fuse element filled into and formed within the interior of a wire channel formed above

a semiconductor substrate in such a way to possess a thin and long flat plane pattern,

A pair of second electroconductors formed in such a way to become contacted with the aforementioned first electroconductor and to possess thin and long flat plane patterns in a state where the respective distal ends thereof oppose one another above the intermediate portion of the aforementioned thin and long first electroconductor, and

A pair of third electroconductors formed respectively above the aforementioned pair of second electroconductors in such a way that they will become contacted with the respective members of the other pair.

Claim 3

A semiconductor device characterized by the possession of

A first electroconductor for a fuse element filled into and formed within the interior of a wire channel formed above a semiconductor substrate in such a way to possess a thin and long flat plane pattern,

A pair of second electroconductors formed in such a way to become contacted with the aforementioned first electroconductor and to possess T-shaped flat plane patterns in a state where the respective upper pattern sides thereof oppose one another while traversing above the intermediate portion of the aforementioned thin and long first electroconductor, and

A pair of third electroconductors formed above the aforementioned pair of second electroconductors in such a way to become contacted with the respective members of the other pair.

Claim 4

A semiconductor device mentioned in Claim 2 characterized by the possession additionally of

An interlayer insulating film constituted to possess a pair of thin and long wire channels filled respectively with the aforementioned pair of second electroconductors and

An etching mask pattern constituted to cover, above the aforementioned interlayer insulating film, the peripheral portions of the aforementioned pair of thin and long wire channels other than the singular mutually opposing respective sides thereof.

Claim 5

A method for manufacturing a semiconductor device characterized by the possession of

A process for depositing a first interlayer insulating film above a semiconductor substrate and for forming a wire channel on a portion of said film,

A process for filling and forming a first electroconductor into and within the interior of the aforementioned wire channel,

A process for forming, above the aforementioned first electroconductor, a capacitor for an anti-fuse constituted to bear a lower metal electrode/insulating film/upper metal

stack structure and to become writable as a result of the electric contact of the aforementioned lower metal with the aforementioned first electroconductor and then of the electric insulation breakdown of the aforementioned insulating film,

A process for depositing a second interlayer insulating film above the semiconductor substrate on which the aforementioned capacitor has been formed and for forming a contact hole on a portion of said film, and

A process for forming a pair of second electroconductors in such a way that will become contacted respectively with the aforementioned first electroconductor and the upper metal electrode of the aforementioned capacitor.

Claim 6

A method for manufacturing a semiconductor device characterized by the possession of

A process for depositing a first interlayer insulating film above a semiconductor substrate and for forming, on a portion of said film, a wire channel in possession of a thin and long flat plane,

A process for filling and forming a wire for a fuse element into and within the interior of the aforementioned wire channel,

A process for depositing a second interlayer insulating film above the aforementioned semiconductor substrate and for forming, on a portion of said film, a pair of thin and long

channels trailing along the aforementioned wire for a thin and long fuse element,

A process for forming a pair of electroconductors for electrodes constituted to become contacted, past the interior of the aforementioned thin and long channel, with the aforementioned wire for a thin and long fuse element in a state where the respective singular edges thereof oppose one another above the intermediate portion of the aforementioned wire for a thin and long fuse element, and

A process for forming a pair of upper metal wire layers in such a way that they will become contacted respectively with the aforementioned pair of electroconductors for electrodes.

Claim 7

A method for manufacturing a semiconductor device characterized by the possession of

A process for depositing a first interlayer insulating film above a semiconductor substrate and for forming, on a portion of said film, a wire channel in possession of a thin and long flat plane,

A process for filling and forming a wire for a fuse element into and within the interior of the aforementioned wire channel,

A process for depositing a second interlayer insulating film above the aforementioned semiconductor substrate and for forming, on a portion of said film, a pair of T-shaped channels each constituted to possess a T-shaped flat plane

pattern in a state where the respective pattern vertical portions thereof trail along the aforementioned wire for a thin and long fuse element and where the respective upper pattern sides thereof oppose one another while traversing above the intermediate portion of the aforementioned wire for a thin and long fuse element,

A process for forming a pair of electroconductors for electrodes filled respectively into the aforementioned T-shaped channels, and

A process for forming a pair of upper metal wire layers in such a way that they will become contacted respectively with the aforementioned pair of electroconductors for electrodes.

Claim 8

A method for manufacturing a semiconductor device mentioned in Claim 6 or 7 characterized by the fact that the aforementioned wire for a fuse element is a polysilicon wire.

Claim 9

A method for manufacturing a semiconductor device characterized by the possession of

A process for depositing a first interlayer insulating film above a semiconductor substrate and for forming, on a portion of said film, a wire channel in possession of a thin and long flat plane,

A process for forming a wire for a thin and long fuse element by filling an electroconductor into the interior of the aforementioned wire channel,

A process for depositing, in proper order, a second interlayer insulating film and a stopper insulating film above the aforementioned semiconductor substrate and for forming, on the aforementioned stopper insulating film, a thin and long hole trailing along the aforementioned wire for a fuse element,

A process for forming a pair of thin and long channels by forming a rectangular etching mask pattern traversing above the intermediate portion of the aforementioned wire for a thin and long fuse element and by selectively etching the aforementioned second interlayer insulating film in relation to the aforementioned stopper insulating film by using said pattern as a mask,

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A process for forming a pair of electroconductors for electrodes constituted to become contacted, past the interior of the aforementioned thin and long channel, with the aforementioned wire for a thin and long fuse element in a state where the respective singular edges thereof oppose one another above the intermediate portion of the aforementioned wire for a thin and long fuse element, and

A process for forming a pair of upper metal wire layers in such a way that they will become contacted respectively with the aforementioned pair of electroconductors for electrodes.

Claim 10

A method for manufacturing a semiconductor device mentioned in Claim 9 characterized by the fact that the aforementioned electroconductor is a polysilicon.

Detailed explanation of the invention

[0001]

(Technical fields to which the invention belongs)

The present invention concerns a semiconductor device semiconductor device constituted to possess an electric fuse element as well as a method for manufacturing the same, and in particular, it concerns a wire structure for feeding a current into an anti-fuse element or fuse element as well as a method for forming the same.

[0002]

(Prior art)

Redundancy techniques designed to substitute defective sites with spare circuits are being practiced extensively for the purpose of improving the production yields of semiconductor devices. On the aforementioned substituting occasions, a method wherein an aluminum wire unit (aluminum fuse) is melt-fractured (laser-blown) by using a laser beam has been often used in the prior art. In recent years, on the other hand, electrically writable fuse elements have captured attention for reasons of small occupant areas, post-packaging substitutabilities, etc.

[0003]

As an embodiment of electric fuse elements, an anti-fuse element of a type for encoding, into a capacitor constituted to possess a structure identical to that of a cell capacitor, information by inducing an electric breakdown of a capacitor insulating film and by mutually conducting capacitor electrodes has, for example, been investigated for DRAMs, although the following problems have been acknowledged.

[0004]

In other words, an electrode equivalent to the accumulation electrode side of a cell capacitor is normally connected to a poly plug or silicon substrate bearing a relatively high resistance, whereas since an anti-fuse capacitor is prepared during a process identical to that for preparing said cell capacitor, a significant voltage drop arises on an occasion for impressing, onto said capacitor, a current and a voltage necessary for the insulation breakdown thereof, and accordingly it becomes necessary to prepare a larger than necessary encoding power source circuit.

[0005]

As another embodiment of electric fuse elements, on the other hand, a fuse element of a wire melt fracture type designed to become melt-fractured as a result of the permeation of an excessive current through a metal wire unit is being investigated, although since the aforementioned metal wire unit is generally designed to bear a low resistance and a high electromigration resistance, it cannot

be easily melt-fractured unless an additional process is introduced anew. A current as high as approximately 10 mA, for example, is deemed necessary for inducing a melt fracture, and in this case, too, a large-scale encoding power source circuit becomes necessary.

[0006]

It may seem feasible to mitigate the aforementioned melt fracture current by using, as a fuse element, a wire bearing a relatively high resistivity (e.g., doped polysilicon, etc.), although the fuse resistance of this element tends to be high, which is problematic in that it cannot be melt-fractured unless a high voltage becomes impressed onto the same.

[0007]

(Problems to be solved by the invention)

As has been mentioned above, anti-fuse elements formed on semiconductor devices of the prior art are connected to current feeding wires via poly plugs or silicon substrates bearing relatively high resistances, which is problematic in that a significant voltage drop arises on an occasion for impressing a current and a voltage necessary for an insulation breakdown and that it becomes necessary to prepare a larger-than-necessary encoding power source circuit.

[0008]

Fuse elements of the wire melt fracture type formed on semiconductor devices of the prior art, furthermore, are

problematic in that a large-scale encoding power source circuit is required since a wire unit cannot be easily fractured.

[0009]

The objective of the present invention, which has been conceived for the purpose of solving the aforementioned problems, is to provide a semiconductor device constituted to possess a fuse element capable of improving the encoding yield and of reducing the occupant area of an encoding power source circuit unit as well as a method for manufacturing the same.

[0010]

(Mechanism for solving the problems)

The first semiconductor device of the present invention is characterized by the possession of a first electroconductor filled into and formed within the interior of a wire channel formed above a semiconductor substrate, a capacitor for an anti-fuse constituted not only to bear an upper metal electrode/insulating film/lower metal stack structure formed above the aforementioned first electroconductor but also to become writable as a result of the electric contact of the aforementioned lower metal with the aforementioned first electroconductor and then of the electric insulation breakdown of the aforementioned insulating film, and a pair of second electroconductors formed respectively above the aforementioned first

electroconductor and above said capacitor in such a way that they will become contacted respectively with the aforementioned first electroconductor and the upper metal electrode of the aforementioned capacitor.

[0011]

The second semiconductor device of the present invention is characterized by the possession of a first electroconductor for a fuse element filled into and formed within the interior of a wire channel formed above a semiconductor substrate in such a way to possess a thin and long flat plane pattern, a pair of second electroconductors formed in such a way to become contacted with the aforementioned first electroconductor and to possess thin and long flat plane patterns in a state where the respective distal ends thereof oppose one another above the intermediate portion of the aforementioned thin and long first electroconductor, and a pair of third electroconductors formed respectively above the aforementioned pair of second electroconductors in such a way that they will become contacted with the respective members of the other pair.

[0012]

Incidentally, it is also conceivable, within the second semiconductor device, to form the aforementioned pair of second electroconductors in such a way that the respective flat planes thereof will possess T-shaped patterns in a state where the respective upper pattern sides thereof oppose one

another while traversing above the intermediate portion of the aforementioned thin and long first electroconductor.

[0013]

Moreover, it is also conceivable for the second semiconductor device to possess, above an interlayer insulating film in possession of a pair of thin and long wire channels filled respectively with the aforementioned pair of second electroconductors, an etching mask pattern constituted to cover the peripheral portions of the aforementioned pair of thin and long wire channels other than the singular mutually opposing respective sides thereof.

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[0014]

The first method of the present invention for manufacturing a semiconductor device is characterized by the possession of a process for depositing a first interlayer insulating film above a semiconductor substrate and for forming a wire channel on a portion of said film, a process for filling and forming a first electroconductor into and within the interior of the aforementioned wire channel, a process for forming, above the aforementioned first electroconductor, a capacitor for an anti-fuse constituted to bear a lower metal electrode/insulating film/upper metal stack structure and to become writable as a result of the electric contact of the aforementioned lower metal with the aforementioned first electroconductor and then of the electric insulation breakdown of the aforementioned

insulating film, a process for depositing a second interlayer insulating film above the semiconductor substrate on which the aforementioned capacitor has been formed and for forming a contact hole on a portion of said film, and a process for forming a pair of second electroconductors in such a way that will become contacted respectively with the aforementioned first electroconductor and the upper metal electrode of the aforementioned capacitor.

[0015]

The second method of the present invention for manufacturing a semiconductor device is characterized by the possession of a process for depositing a first interlayer insulating film above a semiconductor substrate and for forming, on a portion of said film, a wire channel in possession of a thin and long flat plane, a process for filling and forming a wire for a fuse element into and within the interior of the aforementioned wire channel, a process for depositing a second interlayer insulating film above the aforementioned semiconductor substrate and for forming, on a portion of said film, a pair of thin and long channels trailing along the aforementioned wire for a thin and long fuse element, a process for forming a pair of electroconductors for electrodes constituted to become contacted, past the interior of the aforementioned thin and long channel, with the aforementioned wire for a thin and long fuse element in a state where the respective singular edges thereof oppose one another above the intermediate

portion of the aforementioned wire for a thin and long fuse element, and a process for forming a pair of upper metal wire layers in such a way that they will become contacted respectively with the aforementioned pair of electroconductors for electrodes.

[0016]

Incidentally, it is also conceivable, in the course of the second method for manufacturing a semiconductor device, for the aforementioned second interlayer insulating film to possess, in place of a pair of thin and long channels, T-shaped patterns on the respective flat planes thereof, to form a pair of T-shaped channels in a state where the respective pattern vertical portions thereof trail along the aforementioned wire for a thin and long fuse element and where the respective upper pattern sides thereof oppose one another while traversing above the intermediate portion of the aforementioned wire for a thin and long fuse element, and to fill and form, respectively into and within said pair of T-shaped channels, a pair of electroconductors for electrodes.

[0017]

The third method of the present invention for manufacturing a semiconductor device is characterized by the possession of a process for depositing a first interlayer insulating film above a semiconductor substrate and for forming, on a portion of said film, a wire channel in possession of a thin and long flat plane, a process for

forming a wire for a thin and long fuse element by filling an electroconductor into the interior of the aforementioned wire channel, a process for depositing, in proper order, a second interlayer insulating film and a stopper insulating film above the aforementioned semiconductor substrate and for forming, on the aforementioned stopper insulating film, a thin and long hole trailing along the aforementioned wire for a fuse element, a process for forming a pair of thin and long channels by forming a rectangular etching mask pattern traversing above the intermediate portion of the aforementioned wire for a thin and long fuse element and by selectively etching the aforementioned second interlayer insulating film in relation to the aforementioned stopper insulating film by using said pattern as a mask, a process for forming a pair of electroconductors for electrodes constituted to become contacted, past the interior of the aforementioned thin and long channel, with the aforementioned wire for a thin and long fuse element in a state where the respective singular edges thereof oppose one another above the intermediate portion of the aforementioned wire for a thin and long fuse element, and a process for forming a pair of upper metal wire layers in such a way that they will become contacted respectively with the aforementioned pair of electroconductors for electrodes.

[0018]

(Application embodiments of the invention)

In the following, application embodiments of the present invention will be explained in detail with reference to drawings.

[0019]

<First application embodiment>

As the first application embodiment, a structure for connecting, at a low resistance, an anti-fuse and an encoding power source circuit (current feeding source) and a method for forming the same will be explained.

[0020]

Figures 1 (a) through (f), Figures 2 (a) through (d), and Figures 3 (a) through (d) show major processes for manufacturing the memory cell array region and anti-fuse formation region of the DRAM of the first application embodiment of the present invention.

[0021]

First, as Figures 1 (a) and (b) indicate, an element separation region (11) is selectively formed on the surface of a semiconductor substrate (10) based on a technique known in the prior art, and a cell transistor is formed within the memory cell array region of the same, whereas an arbitrary electrode pattern (not indispensable) (13a) is formed above the element separation region (11) of the anti-fuse formation region.

[0022]

Incidentally, (12) in Figures 1 (a) and (b) is a gate insulating film, whereas (13) is the gate electrode of the cell transistor (partially constituting a word line), whereas this gate electrode (13) and the aforementioned electrode pattern (13a) [are each provided by] form[ing] a tungsten silicide (132) above a polysilicon (131), whereas the surface of the same is protected by a gate protective film (14).

[0023]

Within the memory cell array region, furthermore, the graphic display of the source-drain region of the cell transistor is dispensed with for the purpose of simplifying the display, and one pair (two) of cell transistors of an identical row in possession of drains connected commonly to an identical bit line and the cell transistors of the adjacent row are representatively sampled and displayed instead.

[0024]

Next, an interlayer insulating film (15) is deposited by using the lithographic method and RIE method, and the upper portion of the same may, for example, be flattened based on the CMP (chemicomechanical polish) method.

[0025]

Next, as Figures 1 (c) and (d) indicate, aperture units are formed within the memory cell array region at positions scheduled respectively to become a bit line connection unit and a capacitor connection unit, and after polysilicon has been deposited in such a way that fill said aperture units,

the upper portions of the same are removed based, for example, on the CMP method for forming poly plugs (17).

[0026]

Next, as Figures 1 (e) and (f) indicate, an interlayer insulating film (e.g., SiN) (18) is deposited, and bit line wires (e.g., W/TiN) (19) are then formed by using a technique known in the prior art in such a way that they will become contacted respectively with the poly plugs (17) of an identical row for bit line connection. On an occasion for forming said bit line wires (19), it is conceivable to form the same by means of patterning after contact holes have been drilled into portions of the interlayer insulating film (18) and after W has been deposited on the inner planes thereof and above the interlayer insulating film (19) [sic: Presumably "(18)"], although it is also conceivable to form the same by opening bit line wire channels into portions of the interlayer insulating film (18), by opening contact holes

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on portions of the bottom plane of the same, and by filling W into said holes.

[0027]

Next, as Figures 2 (a) and (b) indicate, an interlayer insulating film (e.g., SiN) (20) is deposited, and the upper portion of the same is flattened based, for example, on the CMP method. Next, plug aperture units (21) are opened atop the poly plugs (17) for the capacitor connection unit within the memory cell array region by using the lithographic method

and RIE method, whereas a wire channel (22) is formed atop the aforementioned electrode pattern (13a) within the anti-fuse formation region. In this case, the gate protective film (e.g., SiN) (14) of the anti-fuse formation region serves as a stopper against the RIE.

[0028]

Incidentally, the long diameter/short diameter ratio of the plug aperture unit (21) may, for example, be designated at 2 or below, whereas the long diameter/short diameter ratio of the wire channel (22) may, for example, be designated at 3 or above. Moreover, the plug aperture units (21) are diverted from the bit line wire (19) along the depth direction (anterior and posterior direction in the figure), based on which the severance of the bit line wire (19) is avoided on an occasion for forming the plug aperture units (21).

[0029]

Next, as Figures 2 (c) and (d) indicate, a metal (e.g., tungsten, etc.) is deposited in such a way to fill, via a TiN barrier film (not shown in the figure), for example, the aforementioned plug aperture units (21) and wire channel (22), and the upper portion of the same is then removed based on the CMP method, etc. As a result, metal plugs (23) become formed within the memory cell array region, whereas a metal wire (23a) bearing an extremely large film thickness becomes formed within the anti-fuse formation region.

[0030]

Next, as Figures 3 (a) and (b) indicate, a lower metal (accumulation electrode) (25)/insulating film (high-permittivity film in the present example) (26)/upper metal (plate electrode) (27) structure is formed within the memory cell array region as a cell capacitor (24) of the stack type, whereas an anti-fuse capacitor (24a) constituted to become writable as a result of insulation breakdown on a later occasion is formed within the anti-fuse formation region.

[0031]

These capacitors (24) and (24a) can be formed by using previously disclosed techniques. A thin SiN film (28) and a thick SiO film (not shown in the figure) may, for example, be initially deposited in proper order, and contact holes are then formed on portions of the same (above the conductor of the lower layer).

[0032]

Next, Ru is deposited, as a lower metal (25) on the inner planes of the aforementioned contact holes and above the interlayer insulating film via, if necessary, TiN, for example, and the Ru and the aforementioned SiO film above the aforementioned thick SiO film are then removed. Next, a high-permittivity film (e.g., TaO) (26) is deposited, and after an upper metal (e.g., Ru, etc.) (27) has been further deposited, the upper metal (27) and high-permittivity film (26) are simultaneously patterned.

[0033]

Incidentally, not only singular metals such as Ru, etc. but also metal compounds instantiated, for example, by RuO_2 (ruthenium oxide), $SrRuO_2$ (strontium ruthenium oxide), etc. are usable as metal electrodes.

[0034]

Next, as Figures 3 (c) and (d) indicate, an interlayer insulating film (29) is deposited by using a technique known in the prior art, and after via holes have been formed, upper metal wire layers (30) are formed. On this occasion, a pair of upper metal wire layers (30) are formed within the anti-fuse formation region in such a way that they will become respectively contacted, via contact holes, with the respective singular edges of the upper metal (27) of the capacitor (24a) for an anti-fuse and the metal wire (23a).

[0035]

In other words, according to the aforementioned first application embodiment, an extremely deep wire channel (22) is formed within the anti-fuse formation region by using a wire layer used normally for forming a metal plug (23) within the memory cell array region, and after said channel has been filled with the metal wire (23a), the lower metal (25) of the capacitor (24a) for an anti-fuse is formed in such a way that it will become contacted with one edge portion of said retrieving metal wire (23a), whereas the upper metal wire layers (30) are successively formed, via contact holes, on one edge portion of the retrieving metal wire (23a).

[0036]

As a result, it becomes possible to retrieve the capacitor (24a) for an anti-fuse into the upper metal wire layers (30) without recourse to the intervention of a high-resistance unit indispensable according to embodiments of the prior art such as a diffusion layer within a polysilicon or silicon substrate. It therefore becomes possible to impress a voltage onto the capacitor (24a) for an anti-fuse from the fuse encoding power source circuit via the upper metal wire layers (30) and retrieving metal wire (23a). It becomes possible, on this occasion, to concentrate the encoding electric power exclusively into the anti-fuse portion by inhibiting, at the minimum, the wire resistance from the fuse encoding power source circuit to the capacitor (24a) for an anti-fuse and by inhibiting, at the minimum, the voltage loss incurred in-between the fuse encoding power source circuit and the capacitor (24a) for an anti-fuse.

[0037]

As a result, it becomes possible to improve the encoding yield and to reduce the occupant area of the fuse encoding power source circuit unit, based on which it becomes possible to realize goals of improving the yield of the semiconductor device and of cost depreciation.

[0038]

In other words, the aforementioned first application embodiment is peculiarly characterized by the use, exceptionally for a "retrieving wire" for an anti-fuse unit, of processes used normally for forming contact plugs.

[0039]

It accordingly becomes possible, despite the use of a desirable structure of "capacitor electrode (25)/metal plug (23)/poly plug (17)/cell transistor diffusion layer" within a memory cell array region, to establish, within an anti-fuse formation region, connection with an anti-fuse unit via a path of an extremely low resistance, namely " capacitor electrode (25)/retrieving metal wire (23a)/via contact/upper metal wire layer (30)."

[0040]

In a case where poly plugs are used as retrieval wires for an anti-fuse unit, as in embodiments of the prior art, wires of the 0.13 μm generation, for example, accrue gains of several kΩ due not only to resistances of poly plugs but also to resistances arising in the interface thereof, in contrast with which the metal wire (23a) of the aforementioned first application embodiment can retrieve an anti-fuse unit by accruing a gain of only several tens of Ω.

[0041]

<Second application embodiment>

The second application embodiment pertains to the structure of a fuse element of a type scheduled to become melt-fractured as a result of the permeation of an excessive current through an electroconductive unit.

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[0042]

Figures 4 (a) through (h) and Figures 5 (a) through (c) show major manufacturing processes for the memory cell array region and fuse element formation region of the DRAM of the second application embodiment of the present invention.

[0043]

First, as Figures 4 (a) and (b) indicate, an element separation region (11) is selectively formed on the surface of a semiconductor substrate (10) by using a technique known in the prior art, whereas a cell transistor is formed within the memory cell array region of the same.

[0044]

Incidentally, in Figures 4 (a) and (b), (12) is a gate insulating film, whereas (13) is the gate electrode of the cell transistor (partially constituting a word line), whereas this gate electrode (13) [is provided by] form[ing] a tungsten silicide (132) above a polysilicon (131), whereas the surface of the same is protected by a gate protective film (14).

[0045]

Within the memory cell array region, furthermore, the graphic display of the source-drain region of the cell transistor is dispensed with for the purpose of simplifying the display, and one pair (two) of cell transistors of an identical row in possession of drains connected commonly to an identical bit line and the cell transistors of the adjacent row are representatively sampled and displayed. Next, an interlayer insulating film (15) is deposited, and

the upper portion of the same is flattened based, for example, on the CMP method.

[0046]

Next, as Figures 4 (c) and (d) indicate, aperture units are formed within the memory cell array region at positions scheduled respectively to become a bit line connection unit and a capacitor connection unit by using the lithographic method and RIE method, whereas a wire channel in possession of a thin and long flat plane pattern is formed above the element separation region of the fuse element formation region.

[0047]

An electroconductor (e.g., polysilicon) is then deposited in such a way to fill the aforementioned aperture units and wire channel, and the upper portion of the same is removed based, for example, on the CMP method, as a result of which electroconductive plugs (poly plugs in the present example) (17) become formed within the memory cell array region, whereas, as the plane view diagram of Figure 4 (e) indicates, a wire (17a) for a fuse element in possession of a thin and long flat plane pattern becomes formed above the element separation region of the fuse element formation region.

[0048]

Next, as Figures 4 (f) and (g) indicate, an interlayer insulating film (e.g., SiN) (18) is deposited, and furthermore, a bit line contact hole (36) is formed within

the memory cell array region by using a technique known in the prior art, whereas, as the plane view diagram of Figure 4 (h) indicates, a pair of thin and long channels (36a) trailing along both terminal units of the aforementioned polysilicon wire (17a) for the thin and long fuse element are formed within the fuse element formation region. In this case, the pair of thin and long channels (36a) are formed in such a way to oppose one another via a gap commensurate roughly with the minimal processing dimension (minimal space) above the intermediate portion of the polysilicon wire (17a) for the thin and long fuse element. Incidentally, the long diameter/short diameter ratio of the bit line contact hole (36) may, for example, be designated at 2 or below, whereas the long diameter/short diameter ratio of the thin and long channel (36a) may, for example, be designated at 3 or above.

[0049]

Next, as Figures 5 (a) and (b) indicate, not only are bit line wires (e.g., W/TiN) (19) formed by using the dual damascene method in such a way that they will respectively become connected, past bit wire contact holes (36), with poly plugs (17) of an identical row for bit wire connection but a pair of electrode metal wires (19a) bearing large film thicknesses are also formed, past the thin and long channels (36a), successively to both terminal units of the polysilicon wire (17a) for the thin and long fuse element. Incidentally, in a case where a long polysilicon wire (17a) for a fuse element has been formed, the positions at which the electrode

metal wires (19a) are linked successively to the polysilicon wire (17a) for the fuse element are not limited to both terminal units of the polysilicon wire (17a) for the fuse element.

[0050]

Next, an interlayer insulating film (e.g., SiN) (20) is deposited, and the upper portion of the same is flattened based, for example, on the CMP method. Subsequently, plug aperture units are opened respectively above the poly plugs (17) for the capacitor connection unit within the memory cell array region by using the lithographic method and RIE method, and after a metal such as tungsten, etc. has been deposited via a TiN barrier film (not shown in the figure), for example, in such a way to fill the aforementioned plug aperture units, the upper portions of the same are removed based on the CMP method, etc. As a result, metal plugs (23) become formed within the memory cell array region.

[0051]

Next, an interlayer insulating film inclusive of a thin SiN film (28) is deposited, as has been discussed in the first application embodiment, and a structure of lower metal (accumulation electrode) (25)/insulating film (high-permittivity film in the present example) (26)/upper metal (plate electrode) (27) is formed as a cell capacitor (24) of the stack type within the memory cell array region.

[0052]

Next, an interlayer insulating film (29) is deposited by using a technique known in the prior art, and after via holes have subsequently been formed, an upper metal wire layers (30) are formed. On this occasion a pair of upper metal wire layers (30) are formed, as the plane view diagram of Figure 5 (c) indicates, within the fuse element formation region in such a way that they will become contacted respectively with the pair of electrode metal wires (19a) via contact holes.

[0053]

In other words, it becomes possible, according to the aforementioned second application embodiment, to form a wire unit of a high resistance unused for ordinary wires by using, as a polysilicon wire (17a) for a fuse element, a poly plug (17) layer not normally used as a wire layer.

[0054]

Moreover, it becomes possible, by using, as wires for retrieving a fuse element, electrode metal wires (19a) bearing large film thicknesses and formed simultaneously with a low-resistance bit line contact unit and the bit line wire (19) layer, to retrieve the same at a resistance far lower than those achieved by using ordinary bit lines. According to this method, furthermore, the contact area between the polysilicon wire (17a) for a fuse element and metal wires (19a) for electrodes can be enlarged, which is effective for attenuating the overall resistance of the fuse element retrieval unit.

[0055]

As a result, it becomes possible to impress a voltage in-between both terminal units of the polysilicon wire (17a) for a thin and long fuse element from a fuse encoding (melt-fracturing) power source circuit via upper metal wire layers (30) and wires (19a) for retrieving the fuse element. On this occasion, the resistance of the fuse element alone can be maintained at a high level while inhibiting, at the minimum, the wire resistance from the fuse encoding power source circuit to the fuse element. An encoding (melt-fracturing) action can therefore be easily invoked by effectively

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concentrating, onto the fuse element unit alone, the electric power generated by the fuse encoding power source circuit.

[0056]

<Modified example of second application embodiment>

From the standpoint of concentrating heat generation by effectively concentrating, onto the aforementioned fuse element unit alone, the encoding electric power, it is desirable, as Figure 5 (c) indicates, to up the current density by providing a thin fuse element unit and to concentrate heat generation by forming, above the intermediate portion of a thin and long fuse element unit, a pair of metal wires (19a) for electrodes opposing one another via a gap commensurate roughly with the minimal processing dimension and by concentrating an encoding electric power onto the intermediate portion of the fuse element unit.

[0057]

On an occasion for forming a pair of thin and long channels (36a) scheduled to become filled, via bit line contact layers, with a pair of metal wires (19a) for electrodes in such a way that they will trail along both terminal units of the polysilicon wire (17a) for a thin and long fuse element, however, shortening is likely, as Figure 4 (h) indicates, to arise during a lithographic process since the singular ends (distal ends) of the respective thin and long patterns mutually oppose one another via a gap commensurate with the minimal processing dimension, and therefore, it may become difficult to accurately control the oppositional gap of the respective distal ends at the minimal processing dimension.

[0058]

Instead of forming the thin and long channels (36a), therefore, it is also conceivable, as the plane view diagram of Figure 6 indicates, to form, on the interlayer insulating film (18), a pair of T-shaped channels (36b) constituted to possess T-shaped patterns on the respective flat planes thereof in a state where the respective pattern vertical units thereof trail along both terminal units of the aforementioned polysilicon wire (17a) for a thin and long fuse element and where the respective pattern upper sides thereof oppose one another via a gap commensurate with the minimal processing dimension while traversing above the

intermediate portion of the aforementioned polysilicon wire (17a) for a thin and long fuse element.

[0059]

It becomes possible, by means of such a patterning operation for inducing the mutual opposition of the respective pattern upper sides of T-shaped patterns, to inhibit shortening during a lithographic process and to accurately control the oppositional gap in-between the respective T-shaped patterns.

[0060]

It therefore becomes possible, by filling said pair of T-shaped channels (36b) respectively with a pair of metal wires for electrodes (not shown in the figure), to facilitate an accurate control of the oppositional gap in-between the respective T-shaped patterns (i.e., length of polysilicon portion used as a fuse element). It accordingly becomes possible to inhibit the irregularities of the current value deemed necessary on an occasion for melt-fracturing a fuse element unit and to improve the fuse encoding yield.

[0061]

<Third application embodiment>

Figures 7 (a) through (h) and Figures 8 (a) through (e) show major manufacturing processes of the memory cell array region and fuse element formation region of the DRAM of the third application embodiment of the present invention. The third application embodiment pertains, as in the case of the

second application embodiment, to the structure of a fuse element of a type designed to become melt-fractured as a result of the permeation of an excessive current through an electroconductive unit as well as a method for forming the same, whereas it is peculiarly characterized by the use of self-matching processes as methods for forming bit lines and bit line contacts.

[0062]

First, as the respective cross-sectional view diagrams of Figures 7 (a) through (d) and the plane view diagram of Figure 7 (e) indicate, processes similar respectively to the processes of the second application embodiment shown in Figures 4 (a) through (e) are executed. Components identical to their counterparts of Figures 4 (a) through (e) are hereby designated to bear identical notations for dispensing with overlapping explanations.

[0063]

Next, as Figures 7 (f) and (g) indicate, an interlayer insulating film (18) is deposited, and a stopper insulating film (61) comprising, for example, of a silicon nitride (SiN) film is deposited above the same. Subsequently, a hole (62) for a bit line contact unit is formed on the stopper insulating film (61) within the memory cell array region by using the lithographic method and RIE method, whereas, as the plane view diagram of Figure 7 (h) indicates, a thin and long hole (62a) trailing along the aforementioned wire for a fuse element is formed within the fuse element formation region.

[0064]

Next, as Figures 8 (a) and (b) indicate, a bit line contact hole (66) is formed within the memory cell array region by using the lithographic method and RIE method. On this occasion, a thin and long rectangular etching mask pattern (e.g., SiN) (63) traversing above the intermediate portion of the polysilicon wire (17a) for a fuse element is formed within the fuse element formation region, whereas RIE conditions are designated in such a way to selectively etch the aforementioned interlayer insulating film (18) in relation to the aforementioned stopper insulating film (61) by using said pattern as a mask.

[0065]

As a result, it becomes possible, as the plane view diagram of Figure 8 (c) indicates, to form a pair of thin and long rectangular wire channels (66a) inclusive respectively of both terminal units of the polysilicon wire (17a) for a fuse element. On this occasion, the gap (space) of the mutually opposing pair of thin and long rectangular wire channels (66a) traversing above the intermediate portion of the polysilicon wire (17a) for a fuse element can be controlled, by the aforementioned etching mask pattern (63), to accurately coincide with the minimal processing dimension. Incidentally, the long diameter/short diameter ratio of the aforementioned bit line contact hole (66) may, for example, be designated at 2 or below, whereas the long diameter/short

diameter ratio of the thin and long channel (66a) may, for example, be designated at 3 or above.

[0066]

Next, processes corresponding respectively to their counterparts of the second application embodiment shown in Figures 5 (a) and (b) are executed. In other words, as Figures 8 (d) and (e) indicate, bit line wires (e.g., W/TiN) (19) are initially formed in such a way that they will respectively contacted, via bit line contact holes (66), with poly plugs (17) of an identical row for bit line connection, and furthermore, a pair of metal wires (19a) for electrodes bearing large film thicknesses and linked, via thin and long wire channels (66a), successively to both terminal units of the polysilicon wire (17a) for a thin and long fuse element are formed. Incidentally, the aforementioned etching mask pattern (63) is removed either before or after this process.

[0067]

Next, an interlayer insulating film (20) is deposited, and after the upper portion of the same has been flattened, plug aperture units are opened respectively above poly plugs (17) for the capacitor connection unit within the memory cell array region, and after a metal has been deposited in such a way to fill said plug aperture units, the upper portion of the same is removed based on the CMP method, etc. As a result, metal plugs (23) become formed within the memory cell array region.

[0068]

Next, a structure of lower metal (accumulation electrode) (25)/insulating film (high-permittivity film in

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the present example) (26)/upper metal (plate electrode) (27) is formed as a cell capacitor (24) of the stack type within the memory cell array region.

[0069]

Next, an interlayer insulating film (29) is deposited, and after via holes have been formed, upper metal wire layers (30) are formed. On this occasion, a pair of upper metal wire layers (30) are formed within the fuse element formation region in such a way that they will become contacted, via contact holes, respectively with the pair of metal wires (19a) for electrodes.

[0070]

According to the aforementioned method of the third application embodiment for manufacturing a semiconductor device, the gap (space) of the mutually opposing pair of thin and long rectangular wire channels (66a) traversing above the intermediate portion of the polysilicon wire (17a) for a fuse element can be controlled, by the pair of thin and long rectangular wire channels (66a) and etching mask pattern (63) formed on the stopper insulating film (61), to accurately coincide with the minimal processing dimension.

[0071]

It therefore becomes possible to accurately control the oppositional gap (space) of the pair of metal wires (19a) for

electrodes respectively filled into and formed within the aforementioned pair of thin and long rectangular wire channels (66a). As a result, it becomes possible to inhibit the irregularities of the current value deemed necessary on an occasion for melt-fracturing a fuse element unit and to improve the fuse encoding yield.

[0072]

Incidentally, the semiconductor device obtained in the aforementioned third application embodiment is characterized, in contrast with the semiconductor device obtained in the aforementioned second application embodiment, by the persistence, above the interlayer insulating film (18) in possession of a pair of thin and long wire channels (66a) filled respectively with a pair of metal wires (19a) for electrodes, of an etching mask pattern (61) covering the peripheral portions of the pair of thin and long wire channels (66a) other than the singular mutually opposing respective sides thereof.

[0073]

(Effects of the invention)

As has been discussed above, it becomes possible, according to the present invention, to provide a semiconductor device constituted to possess a fuse element capable of improving the encoding yield and of reducing the occupant area of an encoding power source circuit unit as well as a method for manufacturing the same.

Brief explanation of the figures

Figures 1: Cross-sectional view diagrams partially showing major processes for manufacturing the memory cell array region and anti-fuse formation region of the DRAM of the first application embodiment of the present invention.

Figures 2: Cross-sectional view diagrams partially showing processes following the processes of Figure 1.

Figures 3: Cross-sectional view diagrams partially showing processes following the processes of Figure 2.

Figures 4: Cross-sectional view diagrams and plane view diagrams partially showing major processes for manufacturing the memory cell array region and fuse formation region of the DRAM of the second application embodiment of the present invention.

Figures 5: Cross-sectional view diagrams and a plane view diagram partially showing processes following the processes of Figure 4.

Figure 6: A plane view diagram which shows a partially modified example of the processes of Figure 5.

Figures 7: Cross-sectional view diagrams and plane view diagrams partially showing major processes for manufacturing the memory cell array region and fuse formation region of the DRAM of the third application embodiment of the present invention.

Figures 8: Cross-sectional view diagrams and a plane view diagram partially showing processes following the processes of Figure 7.

(Explanation of notations)

(10): Semiconductor substrate;

(11): Element separation region;

(12): Gate insulating film;

(13): Gate electrode;

(14): Gate protective film;

(15): Interlayer insulating film;

(16) and (16a): Aperture units;

(17): Poly plug;

(18): Interlayer insulating film;

(19): Bit line wire;

(20): Interlayer insulating film;

(21): Plug aperture unit;

(22): Wire channel;

(23): Metal plug;

(23a): Retrieving metal wire;

(24): Cell capacitor;

(24a): Capacitor for anti-fuse;

(25): Lower metal;

(26): Insulating film;

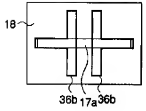
(27): Upper metal;

(28): SiN film;

(29): Interlayer insulating film;

(30): Upper metal wire layer.

Figure 6



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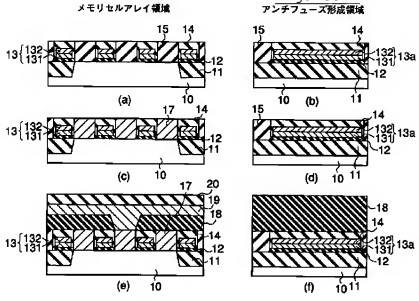
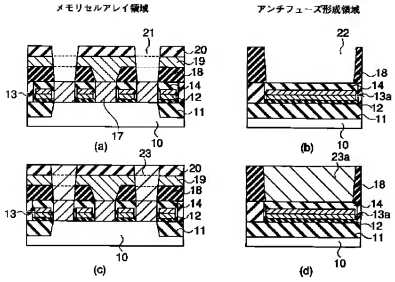
Figures 1



[(A): Memory cell array region; (B): Anti-fuse formation region]

Figures 2



[(A): Memory cell array region; (B): Anti-fuse formation region]

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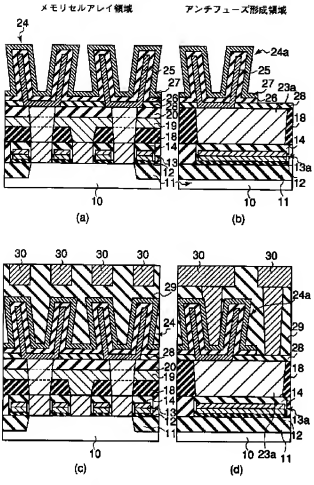
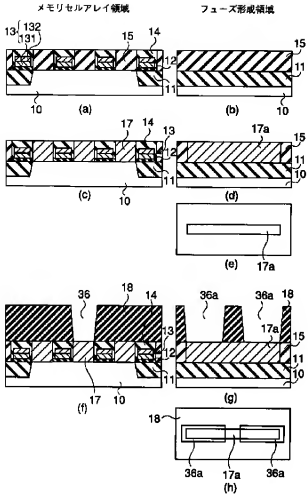
Figures 3



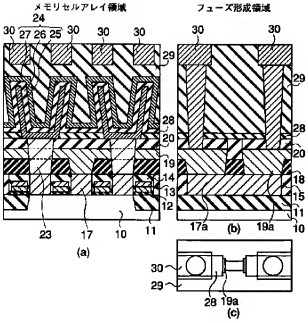
[(A): Memory cell array region; (B): Anti-fuse formation region]

Figures 4



[(A): Memory cell array region; (B): Fuse element formation region]

Figures 5



[(A): Memory cell array region; (B): Fuse element formation region]

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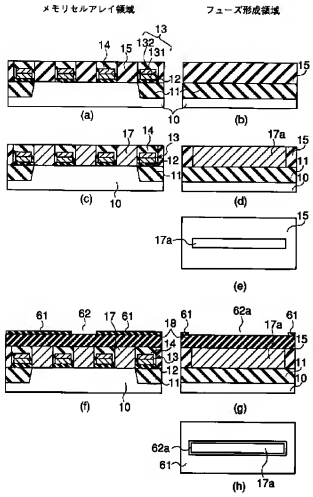
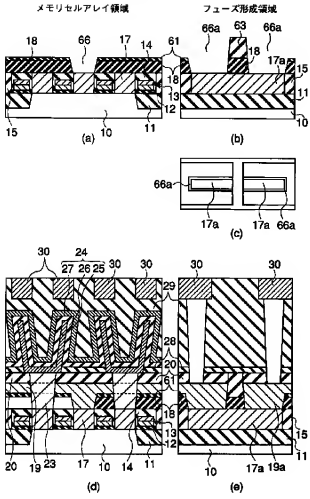
Figures 7



[(A): Memory cell array region; (B): Fuse element formation region]

Figures 8



[(A): Memory cell array region; (B): Fuse element formation region]